OIPE
FEB 27 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:)
)
    M. EROZ et al.   )   Group Art Unit: 2133
)
)   Examiner: Not Yet Assigned
Application No: 10/613,823   )
)
Filed: July 3, 2003   )
)   February 26, 2004
)
Title: METHOD AND SYSTEM FOR   )
      PROVIDING LOW DENSITY PARITY   )
      CHECK (LDPC) ENCODING   )
)

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Special Program Examiner GAU

PETITION TO MAKE SPECIAL PURSUANT TO 37 C.F.R. § 1.102

Dear Sir:

    Applicants respectfully petition the Commissioner to advance examination of this application pursuant to the provisions of 37 C.F.R. § 1.102(d) and MPEP 708.02 (VIII). An Information Disclosure Statement, including a Form 1449 and a copy of each reference cited therein, accompanies this Petition.

VIII. (A) The Commissioner is hereby authorized to charge Deposit Account No. 50-0383 $130 for a Petition to Make Special in accordance with 37 C.F.R. 1.17(h). Should the Commissioner determine that an additional fee is due, he is hereby authorized to charge the additional fee to Deposit Account 50-0383.

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CONCLUSION

It is respectfully requested that examination of the above-referenced application be advanced in accordance with the provisions of 37 C.F.R. § 1.102 and MPEP 708.02.

Applicants' undersigned attorney may be reached by telephone at (301) 601-7252. All correspondence should continue to be directed to our address given below.

Respectfully submitted,

February 26, 2004

Craig L. Plastrik
Registration No. 41,254

Hughes Electronics Corporation
Customer No. 20991

VIII. (B) All of the claims presented in the above-identified patent application are believed to be directed to a single invention. If the Examiner believes that the pending claims are directed to more than one invention, Applicants hereby agree to elect claims directed to a single invention, without traverse.

The present invention is directed to a method and system for encoding structured Low Density Parity Check (LDPC) codes. LDPC codes are a class of block error control codes that allow a communication system to approach the Shannon limit, which is the theoretical upper limit for data rate at a given signal to noise ratio. However, LDPC codes have not been widely deployed commercially because of their complexity and because very large blocks are required for effective use, thus causing storage problems. Therefore, it is an objective of the present invention to provide an LDPC communication system that employs simple encoding and decoding processes.

The present invention addresses this objective by providing a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

VIII. (C) A pre-examination search was conducted by a professional search firm. The search was conducted in Class 375, subclasses 259, 261, 265, 268, 269, 272, and 279; Class 714, subclasses 752, 758, 781, and 782; and on computer using Delphion, EPO ESPACE, and PTO databases; and on the Internet. In addition, an International Search Report for corresponding International Patent Application No. PCT/US03/21073 has been issued by the European Patent Office acting as the International Search Authority.

VIII. (D) The pre-examination search revealed the following references:

(i) U.S. Patent No. 6,567,465

(ii) U.S. Patent Application Publication No. US 2003/0203721 A1

(iii) U.S. Patent Application Publication No. US 2003/0187899 A1

(iv) U.S. Patent Application Publication No. US 2003/0014718 A1

(v) International Publication No. WO 03/088504 A1

(vi) International Publication No. WO 03/065591 A2

Each of these references is included in the Information Disclosure Statement, along with a copy of each reference.

The International Search Report cited the following additional references:

(vii) European Patent Application No. EP 1 093 231 A1

(viii) International Publication No. WO 02/099976 A2

(ix) S. Johnson et al., "Construction of Low-Density Parity-Check Codes from Kirkman Triple Systems", Proceedings, IEEE Global Telecommunications Conference 2001, pp. 970-974, November 25-29, 2001

(x) T. Richardson et al., "Efficient Encoding of Low-Density Parity Check Codes", IEEE Transactions on Information Theory, Vol. 47, No. 2, pp. 638-656, February 2001

(xi) L. Ping et al., "Low Density Parity Check Codes with Semi-Random Parity Check Matrix", Electronics Letters, IEE Stevenage, Vol. 35, No. 1, pp. 38-39, January 7, 1999

(xii) B. Vasic et al, "Kirkman Systems and Their Application in Perpendicular Magnetic Recording", IEEE Transactions on Magnetics, Vol. 38, No. 4, pp. 1705-1710, July 2002

(xiii) R. Echard et al., "The Pi-Rotation Low-Density Parity Check Codes", Proceedings, IEEE Global Telecommunications Conference 2001, pp. 980-984, November 25-29, 2001

(xiv) B. Vasic, "Combinatorial Constructions of Low-Density Parity Check Codes for Iterative Decoding", Proceedings, IEEE International Symposium on Information Theory 2002, p. 312, June 30-July 5, 2002

(xv) B. Vasic, "Structured Iteratively Decodable Codes Based on Steiner Systems and Their Application in Magnetic Recording", Proceedings, IEEE Global Telecommunications Conference 2001, pp. 2954-2960, November 25-29, 2001

Each of these references is included in the Information Disclosure Statement, along with a copy of each reference. A copy of the International Search Report is also included with the Information Disclosure Statement.

VIII. (E) A discussion of the above-listed references is provided below:

(i)   United States Patent No. 6,567,465 relates to a DSL modem with a received and a transmitter that includes an LDPC encoder which utilizes a generation matrix G which is derived from a substantially deterministic H matrix in order to generate redundant parity bit for a block of bits. The H matrix is determined by assigning "ones" of a first column N_j randomly or deterministically. Then, beginning with the second column, assignment of "ones" is carried out deterministically with each "one in a previous ancestor column generating a "one" in the next descendant column based on the rule that a descendant is placed one position below or above an ancestor. As a result, descending or ascending diagonals are generated. When distributing "ones" in any given column, care is taken to ensure that no rectangles are generated in conjunction with other "ones" in the current column and previous columns. By avoiding generation of rectangles, diagonals are interrupted.

United States Patent No. 6,567,465, however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC

coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(ii)   United States Patent Application Publication No. US 2003/0203721 relates to a method for generating an adaptive air interface waveform that comprises generating a waveform that include a variable carrier frequency and variable bandwidth signal. The variable bandwidth signal includes one or more subcarriers that are dynamically placeable over a range of frequencies, and each subcarrier is separately modulated according to a direct sequence spread spectrum technique. The waveform has an embedded pilot usable to optimize one or more spectrum efficiencies of the waveform. A modulation constellation, a code rate, and a code length of the generated wavefor are adapted according to an available spectrum and one or more sub-carrier conditions.

United States Patent Application Publication No. US 2003/0203721, however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(iii)   United States Patent Application Publication No. US 2003/0187899 relates to a matrix operation processing device. In the device, an input signal data string is temporarily stored in a register, and is input to an adder according to the instruction of a control unit. The control unit designates a ROM storing a check matrix H and obtains information about a position, in which 1 is stored in a specific column of the check

matrix. The ROM instructs SEL1#1 through #CW to select a value corresponding to the position, in which the check matrix is 1 from values from reg(M) using a selector SELL and sends it to an adder. If the result of an addition is selected by a selector SEL2 instructed to select it by the ROM, then it is input to the reg(M). If no addition has been applied, the value output from the reg(M) is input to the reg(M) through the selector SEL2. This process is repeated until all the operations have finished.

United States Patent Application Publication No. US 2003/0187899, however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(iv)   United States Patent Application Publication No. US 2003/0014718 relates to a computer-implemented system and method for generating LDPC codes. One aspect includes a method for generating high rate LDPC codes that first constructs a matrix H of size mxn having m rows of check nodes and n columns of bit nodes. The matrix meets the following requirements: the weight of the jth column equals a_j; each row, r has weight at most b_r; and the matrix H can be represented by a Tanner graph that has girth of at least g greater than or equal to g. The method then iteratively adds an $(n+1)^{th}$ column U_1 to matrix H, wherein the size of U_1 is initially empty and is at most a_{n+1}, and wherein U_1 comprises a set of i check nodes such that i is greater than or equal to zero and i is less than a_{n+1}. The method then iteratively adds check nodes to U_1 such that each check node does not violated predetermined girth and check-degree constraints. The matrix H is updated when a new column is added. The iterations are terminated if

there are no new check nodes that do not violate the girth and check-degree constraints. The method can be modified to optimize various parameters, including the following cases: maximizing the rate for a fixed girth; maximizing the girth for a fixed rate; and maximizing the rate for a fixed girth and a fixed length.

United States Patent Application Publication No. US 2003/0014718, however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(v)   International Publication No. WO 03/088504 relates to a method for decoding error correcting codes, wherein a decoded data block is associated with coded data according to a global code comprising at least two sub-codes. An irregular bipartite graph is associated with the global code, the decoding method is iterative, and a data block to be decoded is distributed between a plurality of disjointed memory banks which can be independently addressed. The method also comprises, at each iteration, a stage for feeding in parallel at least two decoders which respectively correspond to at least one of the sub-codes, in terms of the data to be decoded, the data to be decoded being extracted in parallel from at least two of the memory banks in order to feed the same amount of decoders, and each decoder is sequentially fed with the data to be decoded corresponding thereto. The publication also relates to a corresponding coding method, corresponding coding/decoding devices, and a corresponding signal.

International Publication No. WO 03/088504, however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing

information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(vi)   International Publication No. WO 03/065591 relates to a method and apparatus for decoding digital information transmitted through the communication channel or recorded on a recording medium. The method and apparatus are preferably applied in the systems where data is encoded using regular LDPC codes with parity check matrices composed from circulants (a matrix is called a circulant if all of its columns or rows are cyclic shifts of each other).

International Publication No. WO 03/065591, however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(vii)   European Patent Application No. 1 093 231 relates to a construction method for LDPC codes, and simple systematic coding of LDPC codes. The LDPC coding

procedure codes M information symbols with N-M redundant (i.e., parity check) symbols which has the same minimum number of nonzero elements in each row and less than two rows or columns with only one nonzero value.

European Patent Application No. EP 1 093 231, however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(viii)   International Publication No. WO 02/099976relates to a method of generating low density parity check codes for encoding data that includes constructing a parity check matrix H from a balanced incomplete block design in which a plurality of B-sets which define the matrix have no more than one intersection point. The parity bits are then generated as a function of the constructed parity check matrix H.

International Publication No. WO 02/099976, however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein

the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(ix)   The article entitled "Construction of Low-Density Parity-Check Codes from Kirkman Triple Systems" by Johnson et al. relates to a construction method for regular LDPC codes based on combinatorial designs known as Kirkman triple systems. The authors have observed that analytically constructed LDPC codes comprise only a very small subset of possible codes, and as result, most LDPC codes are constructed randomly. An approach is shown for constructing (3,p)-regular codes whose Tanner graph is free of 4-cycles for any integer p.

The article entitled "Construction of Low-Density Parity-Check Codes from Kirkman Triple Systems," however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(x)   The article entitled "Efficient Encoding of Low-Density Parity-Check Codes" by T. Richardson et al. relates to the encoding problem for LDPC codes, and more generally to the encoding problem for codes specified by sparse parity-check matrices. An approach for exploiting the sparseness of the parity-check matrix to obtain efficient encoders is presented. For the (3,6)-regular LDPC code, for example, the complexity of encoding is essentially quadratic in the block length. However, it is shown that the associated coefficient can be made quite small, so that encoding codes even of length

n ≈ 100,000 is still quite practical. It is also shown that "optimized" codes actually admit linear time encoding.

The article entitled "Efficient Encoding of Low-Density Parity-Check Codes," however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(xi)   The article entitled "Low Density Parity Check Codes with Semi-Random Parity Check Matrix" by L. Ping et al. relates to a semi-random approach to LDPC code design. The presented approach is shown to achieve essentially the same performance as an existing method, but with considerably reduced complexity.

The article entitled "Low Density Parity Check Codes with Semi-Random Parity Check Matrix," however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(xii)   The article entitled "Kirkman Systems and Their Application in Perpendicular Magnetic Recording" by B. Vasic et al. relates to an introduction of a novel class of very high-rate LDPC codes. This class of codes is investigated in the context of its application in a perpendicular magnetic recording system. New codes are well structured and, unlike random codes, can lead to a very low-complexity implementation. A systematic way of constructing codes is based on Kirkman systems. A hardware-efficient encoding algorithm is proposed. The bit error rate characteristics are characterized by simulation of the soft iterative decoding in perpendicular magnetic read channel with different partial response targets and types of noise.

The article entitled "Kirkman Systems and Their Application in Perpendicular Magnetic Recording," however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(xiii)   The article entitled "The Pi-Rotation Low-Density Parity Check Codes" by R. Echard et al. relates to an introduction of an ensemble of quasi-regular LDPC error control codes called pi-rotation LDPC codes. These codes are completely defined by a single permutation vector of length $n/8$, where n is the length of the code. An efficient coding scheme and circuit design based on the single permutation are presented. Simulation results indicate that these codes perform as well as regular LDPC codes

based on completely random matrix constructions. These features make the pi-rotation code valuable for practical communication system implementation.

the article entitled "The Pi-Rotation Low-Density Parity Check Codes," however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(xiv)   The article entitled "Combinatorial Constructions of Low-Density Parity Check Codes for Iterative Decoding" by B. Vasic relates to a method for a combinatorial construction of regular LDPC codes based on balanced incomplete block designs, or more specifically on cyclic difference families of Abelian groups and affine geometries. Several constructions are presented, and the bounds on minimal distance are derived by using the concept of Pasch configurations.

The article entitled "Combinatorial Constructions of Low-Density Parity Check Codes for Iterative Decoding," however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC

coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

(xv)   The article entitled "Structured Iteratively Decodable Codes Based on Steiner Systems and Their Application in Magnetic Recording" relates to a method for a combinatorial construction of a class of iteratively decodable codes, an approach diametrically opposed to the prevalent practice of using large, random-like codes. These codes are well-structured and, unlike random codes, can lend themselves to a very low complexity implementation. A systematic way of constructing codes based on Steiner systems and the Zv group is presented, and a hardware-efficient encoding algorithm is proposed. A substantial performance improvement of high-rate Steiner codes over the existing schemes used in magnetic recording systems is demonstrated.

The article entitled "Structured Iteratively Decodable Codes Based on Steiner Systems and Their Application in Magnetic Recording," however, fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; retrieving the stored information representing the parity check matrix to output an LDPC coded signal; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.